WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising: a six-transistor memory cell; and a word line and a pair of bit lines, the word line and the pair of bit lines being connected to the memory cell,

the semiconductor memory device further comprising:

means for precharging the pair of bit lines to a power source voltage;

a dummy bit line different from the pair of bit lines;

means for discharging the dummy bit line to a first voltage lower than the power supply voltage; and

means for equalizing the pair of bit lines precharged to the power source voltage and the dummy bit line discharged to the first voltage to set the voltages on the pair of bit lines before read operation of the memory cell at a second voltage lower than the power supply voltage.

2. The semiconductor memory device of claim 1, wherein the dummy bit line is placed between the pair of bit lines.

3. The semiconductor memory device of claim 1, including means for electrically dividing the dummy bit line into at least two.

4. The semiconductor memory device of claim 3, including means for changing the number of divisions of the dummy bit line.

5. The semiconductor memory device of claim 1, including means for controlling the first voltage on the dummy bit line to change the second voltage on the pair of bit lines.

6. The semiconductor memory device of claim 5, including means for changing a substrate potential of an MOS transistor for drawing charge from the dummy bit line when the dummy bit line is discharged.

7. A semiconductor memory device, comprising: a six-transistor memory cell; and a word line and a pair of bit lines, the word line and the pair of bit lines being connected to the memory cell,

the semiconductor memory device further comprising:

means for precharging the pair of bit lines to a power supply voltage; and

means for discharging the pair of bit lines precharged to the power supply voltage for a given period of time to set the voltage on the pair of bit lines before read operation of the memory cell at a given voltage lower than the power supply voltage.

8. The semiconductor memory device of claim 7, including means for equalizing voltages on the pair of bit lines in both a precharging time and a discharging time of the pair of bit lines.

9. The semiconductor memory device of claim 7, including means for changing a discharging time of the pair of bit lines.

10. A semiconductor memory device, comprising: a six-transistor memory cell; and a word line and a pair of bit lines, the word line and the pair of bit lines being connected to the memory cell,

the semiconductor memory device further comprising: means for setting an

activation voltage on the word line in read operation of the memory cell at a given voltage lower than a power supply voltage.

11. The semiconductor memory device of claim 10, including means for changing the activation voltage on the word line.